LISTING OF CLAIMS:

1. (Currently amended) A receiver comprising:

analog-to-digital circuitry for generating a digital representation, comprising a bit signal, of an amplified analog signal at an input;

adjustable gain control circuitry for receiving a radio signal and outputting the amplified analog signal using a gain determined connected directly to ~~a~~ the bit signal at an output of the analog-to-digital circuitry; ~~and~~

digital channel filtering circuitry for filtering said digital representation; and

digital processing circuitry for processing the output of said digital channel filtering circuitry,

wherein the gain is adjusted by a first amount responsive to a first bit selected from a plurality of most significant bits in the bit signal, the first bit indicating that the output of the analog-to-digital circuitry has exceeded a first threshold,

wherein the gain is adjusted by a second amount responsive to a first set of bits selected from the plurality of most significant bits in the bit signal, the first set of bits indicating that the output of the analog-to-digital circuitry has exceeded a second threshold,

wherein the first amount is not equal to the second amount, and

wherein the first threshold is not equal to the second threshold.

2-3. (Canceled)

4. (Currently amended) The receiver of claim ~~3~~ 1 wherein said adjustable gain control circuitry ~~reduces~~ adjusts said gain independent of said digital processing circuitry.

5. (Canceled)

6. (Currently amended) The receiver of claim ~~2-1~~ 1 wherein said gain is ~~increased~~ adjusted by a third amount responsive to a second set of bits selected from the plurality of most significant bits of said bit signal, the second set of bits indicating that the output of the analog-to-digital ~~converter~~ circuitry is below a third threshold.

7. (Currently amended) A method of receiving a signal in a receiver, comprising the steps of:

generating a digital representation of a signal at an output of an analog-to-digital converter after applying a gain to the signal;

adjusting the gain by a control directly connected and responsive to bit values of the digital representation of said output of said analog-to-digital converter;

generating a filtered digital representation for a desired channel; and

processing the filtered digital representation,

wherein adjusting the gain comprises

adjusting the gain by a first predetermined amount responsive to a first bit selected from a plurality of most significant bits from the bit values of the digital representation, the first bit indicating that the output of the analog-to-digital converter has exceeded a first threshold, and

adjusting the gain by a second predetermined amount responsive to a first set of bits selected from said plurality of most significant bits from the bit values of the digital representation, the first set of bits indicating that the output of the analog-to-digital converter has exceeded a second threshold,

wherein the first predetermined amount and the second predetermined amount are not equal, and

wherein the first threshold is not equal to the second threshold.

8-12. (Canceled)

13. (Currently amended) A receiver comprising:

adjustable gain control circuitry for receiving a radio signal and outputting an amplified analog signal using a gain connected directly to a single bit sample of a digital representation signal at an output of an analog-to-digital ~~(ADC)~~ circuitry;

digital channel filtering circuitry for filtering said digital representation; and

digital processing circuitry for processing the output of said digital channel filtering circuitry,

wherein the gain is operable to be adjusted by a first amount responsive to a first bit selected from a plurality of most significant bits in the single bit sample of the digital representation signal, the first bit indicating that the output of the analog-to-digital circuitry has exceeded a first threshold,

wherein the gain is operable to be adjusted by a second amount, responsive to a first set of bits selected from the plurality of most significant bits in the single bit sample of the digital representation signal, the first set of bits indicating that the output of the analog-to-digital circuitry has exceeded a second threshold,

wherein the first amount and the second amount are not equal, and

wherein the first threshold is not equal to the second threshold.

14. (Previously presented) The receiver of claim 13 wherein said adjustable gain control circuitry is coupled to receive an output signal from at least one low pass filter.

15. (Previously presented) The receiver of claim 14 wherein at least one input of said at least one low pass filter is coupled to an output of at least one mixer.

16. (Previously presented) The receiver of claim 15 wherein at least one input of said at least one mixer is coupled to an output of an amplifier.

17. (Previously presented) The receiver of claim 16 wherein an input of said amplifier is coupled to an output of a bandpass filter.

18. (Previously presented) The receiver of claim 14 wherein said at least one low pass filter comprises two low pass filters.

19. (Previously presented) The receiver of claim 13 wherein said adjustable gain control circuitry comprises two gain control circuits, whereby both sensitivity and interference tests may be conducted.

20. (Currently amended) The receiver of claim 13 wherein at least ~~an MSB bit~~ one bit from the plurality of most significant bits in the single bit sample of said digital representation at said output of the analog-to-digital circuitry is directly connected to an input of said adjustable gain control circuitry.

21. (Previously presented) The receiver of claim 13 wherein said analog-to-digital circuitry comprises two analog-to-digital circuits, one of said analog-to-digital circuits having an output directly connected to an input of said adjustable gain control circuitry, whereby both sensitivity and interference tests may be conducted.

22-24. (Canceled)

25. (Currently amended) The receiver of claim 1 wherein ~~said gain is reduced by a first amount responsive to a most significant of said bit signal~~ the first bit is the most significant bit of the plurality of most significant bits, the first bit indicating that the output of the analog-to-digital converter has exceeded ~~a~~ the first ~~saturation~~ threshold, and wherein the ~~most significant of said~~ first bit signal is directly connected to a gain control input of the adjustable gain control circuitry.

26. (Currently amended) The receiver of claim 1 wherein said gain is ~~set~~ adjusted by the first amount using ~~by~~ the output of the analog-to-digital circuitry ~~(ADC)~~ without ~~DSP~~ intervention from the digital processing circuitry if the output of the ~~ADC~~ analog-to-digital circuitry is close to saturation over ~~a~~ the first threshold.

27. (Currently amended) The method of claim 7 wherein said adjusting the gain by the first predetermined amount is performed using ~~set by~~ the output of the analog-to-digital converter ~~(ADC)~~ without ~~DSP~~ intervention from a digital processor if the output of the ~~ADC~~ analog-to-digital converter is close to saturation over ~~a~~ the first threshold.

28. (Currently amended) The receiver of claim 13 wherein said gain is ~~set~~ operable to be adjusted by the first amount using the output of the ~~ADC~~ analog-to-digital circuitry without ~~DSP~~ intervention from the digital processing circuitry if the output of the ~~ADC~~ analog-to-digital circuitry is close to saturation over ~~a~~ the first threshold.

29. (New) The receiver of claim 1 wherein both the first and the second amounts represent a decrease in the gain.

30. (New) The receiver of claim 6 wherein the third amount represents an increase in the gain.

31. (New) The method of claim 7 wherein both the first and second predetermined amounts represent a decrease in the gain.

32. (New) The method of claim 7 wherein adjusting the gain further comprises adjusting the gain by a third amount responsive to a second set of bits selected from the plurality of most significant bits from said bit values of the digital representation, the second set of bits indicating that the output of the analog-to-digital converter has fallen below a third threshold.

33. (New) The method of claim 32 wherein the third amount represents an increase in the gain.

34. (New) The receiver of claim 13 wherein the both first and second amounts represent a decrease in the gain.

35. (New) The receiver of claim 13 wherein the gain is operable to be adjusted by a third amount responsive to a second set of bits selected from the plurality of most significant bits in the single bit sample of the digital representation signal, the second set of bits indicating that the output of the analog-to-digital circuitry has fallen below a third threshold.